Notice of Allowability	Application No.	Applicant(s)	
	09/576,056	BALLINGER, DAVID GORDON	
	Examiner	Art Unit	
	Sudhanshu C. Pathak	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *May 26th, 2005*.

2. ☒ The allowed claim(s) is/are *45-53, 55-62 & 65-68 and renumbered as claims 1-21-*.

3. ☒ The drawings filed on *April 16th, 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948).attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 45-53, 55-62 & 65-68 are pending in the application.

2. Claims 1-44, 54, 63-64 & 69 have been canceled.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Aslam A. Jaffery on June 22nd, 2005.

- In order to avoid a "Prior Art" rejection the claims have been amended as follows:
  - In Claim 55, line 7 **replace** "synchronizing a bit clock by using the history of correlation; and" **with**

    .....generating and synchronizing a bit clock; .....
  - In Claim 55, line 11 **replace** "corresponding counter." **with**

    ..... corresponding counter over all possible sample positions for the bit clock; and

    wherein the generating and synchronizing a bit clock includes using the histogrammed correlator output to select / adjust the sample positions for the bit clock to a position where the corresponding correlation exceeds the threshold. .....

- In Claim 56, line 7 **replace** "synchronizing a bit clock by using the history of correlation; and" **with**

  .....generating and synchronizing a bit clock; .....

- In Claim 56, line 13 **replace** "for the bit clock." **with**

  .....for the bit clock; and

  wherein the generating and synchronizing a bit clock includes using the histogrammed correlator output to select / adjust the sample positions for the bit clock to a position where the corresponding correlation exceeds the threshold. .....

Allowable Subject Matter

4. Claims 45-53, 55-62 & 65-68 and renumbered as claims 1-21 respectively are allowable over the prior art of record because the cited references do not contain the specified limitation of a pseudo-noise encoded digital data clock recovery circuit for recovering an original bit stream from a received chip stream, comprising:

a correlator to correlate a pseudo-noise sequence with the received chip stream and generating a correlator output, the pseudo-noise sequence to modulate the original bit stream;

a phase controller, coupled to the correlator to histogram the correlator output of the correlator over the plurality of bit periods, wherein the phase controller includes a plurality of counters to histogram the correlator output over all sample positions in a bit period for the plurality of consecutive bit periods, each of the counters

corresponding to each of the sample positions within the bit period and, wherein each of the counters is incremented when a corresponding thresholded correlator output generates a spike at the corresponding sample position; and

a bit clock generator, coupled to the phase controller, to generate a bit clock which determines a sampling position of the received chip stream to recover the original bit stream from the received chip stream, the bit clock generator to use the histogram of the correlator output to select/adjust the sample position for the bit clock, wherein the bit clock generator adjusts the sample position of the bit clock to a position where the corresponding counter exceeds a threshold and, wherein the bit clock generator retains the same sample position of the bit clock where no counters exceed the threshold.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sudhanshu C. Pathak whose telephone number is (571)-272-3038. The examiner can normally be reached on M-F: 9am-6pm.

    - If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571)-272-3056
    - The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

- Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Sudhanshu C. Pathak

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